AMENDMENT TO THE DRAWINGS

Please replace the drawing sheets for FIGS. 2B and 3 with the attached Replacement Drawing Sheets.

Attachments.

REMARKS

Claims 1, 4-14, and 16-29 are pending in this application. Claims 1, 14, 21 and 27 are amended. Claims 2, 3, and 15 have been canceled by a previous amendment. In the Office Action, claims 1, 4-14, and 16-29 are rejected over prior art. Reconsideration of the rejection is respectfully requested.

DRAWING OBJECTIONS

Applicants are of the belief that replacement sheets for FIGS. 2B and 3 have already been filed in response to the drawing objections of October 19, 2005. Regardless, Applicants again submit replacement sheets for FIGS. 2B and 3.

CLAIM REJECTION UNDER 35 U.S.C. §102

Claims 1, 4, 8, 12 and 21-22 are rejected under 35 U.S.C. § 102(b) as being anticipated by Horisaki et al. (JP 2001-155497). The rejection is respectfully traversed.

The Examiner alleges that Horisaki et al. teaches "uploading an integrated burn-in test program to the burn-in equipment for testing the multi-chip package," at the last 4 lines of paragraph [0006]. The Examiner further alleges that at paragraph [0009], Horisaki et al. teaches the multiple kinds of semiconductor devices include at least one of NVM, SRAM, and DRAM.

However, the two sections cited by the Examiner only teach that semiconductor memory devices include classes in DRAM, SRAM, and FLASH. In other words, there is no suggestion or teaching of an integrated burn-in test nor teaching of a multiple kinds of semiconductor devices including at least one of NVM, DRAM, and SRAM. Horisaki et al. only teaches test

equipment having a burn-in test suited for one of a memory device in the class of DRAM, SRAM, and FLASH. Applicants submit that Horisaki et al., at best, teaches the prior art disclosed in the background of the present application.

To better distinguish the present claims over the Horisaki et al. reference, Applicants have amended independent claims 1, 14, 21 and 27. Specifically, the claims have been similarly amended to clarify that a multi-chip package includes semiconductor devices having at least two of a non-volatile memory, a SRAM, and a DRAM.

As discussed above, Horisaki et al. only teaches testing **one** of DRAM, SRAM, and FLASH using a **single** burn-in test program. Horisaki et al. fails to teach all the features of independent claims 1 and 21. For at least the reasons given above, claims 1 and 21 are patentable over Horisaki et al. Dependent claims 4, 8, 12, and 22 are also patentable for depending on respective allowable base claim.

Claims 1, 14, 16-17, 20-21, 27 and 19 are rejected under 35 USC 102(b) as being anticipated by Tom et al. [sic] (MCM BURN-N EXPEREINCE). The rejection is respectfully traversed.

The Examiner basically alleges that section III discloses all the features recited in independent claims 1, 14, 21, and 27. For brevity, Applicants will discuss similarly recited independent claims 1, 14, 21, and 27 collectively.

First, nowhere in section III of Tom et al. [sic] does it disclose uploading an **integrated** burn-in test **program,** as alleged by the Examiner. Section III only discloses that a burn-in test is conducted on a MCM. There is no suggestion or teaching that a burn-in test **program** is used, nor is it inherent that a program is used to for the burn-in test. A burn-in test may be conducted

manually. Section V of Tom et al. [sic] discloses a burn-in tool, but nowhere does it disclose that the burn-in tool uses an integrated burn-in test program.

In addition, Tom et al. [sic], at best, discloses testing a CMOS chip, as recognized by the Examiner in his rejection with respect to claim 16. Tom et al. [sic] fails to suggest or teach a burn-in test with an integrated program and also fails to suggest or teach a multiple kinds of semiconductor devices including at least two of NVM, DRAM, and SRAM.

For at least the reasons given above, independent claims 1, 14, 20, and 27 are patentable over Tom et al. [sic]. Dependent claims 16-17, 21, and 29 are also patentable for depending on respective allowable base claim.

CLAIM REJECTION UNDER 35 U.S.C. §103

Claims 5-7, 9-11, 13, 19, 23-26 and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Horisaki et al. in view of APA in further view of Eide (U.S. Patent 6,014,316). This rejection is also respectfully traversed.

As discussed above, Horisaki et al. neither suggest nor teaches the features recited in independent claims 1, 14, 21 and 27. In addition, the APA nor Eide cure the deficiencies of Horisaki et al. Therefore, respective dependent claims 5-7, 9-11, 13, 19, 23-26 and 28 are also patentable for depending on respective allowable base claim.

CONCLUSION

In view of the above remarks, reconsideration of the rejections and allowance of claims 1, 4-14 and 16-29 are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If the Examiner believes that a personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (703) 668-8000.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, PLC

By_____
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